In The Claims:

Claims 1-8 (canceled)

9. (original) A semiconductor device, comprising:

a substrate;

a gate structure on said substrate, said gate structure including a gate dielectric layer on said substrate and a gate conductive layer on said gate dielectric layer;

an oxide spacer on a sidewall of said gate structure;

a spacer on said oxide spacer;

a source/drain region in said substrate besides said gate structure and said spacer; and

an offset oxide layer on said substrate and said source/drain region, said offset oxide layer having a bottom surface below a bottom surface of said gate dielectric layer.

10. (original) The device of claim 9, wherein a material of said oxide spacer includes silicon oxide.

11. (original) The device of claim 9, wherein a material said spacer includes silicon nitride.

12. (original) The device of claim 9, wherein said oxide spacer has an etching selectivity relative to said spacer.

13. (original) The device of claim 9, further comprising a source/drain extension region below said oxide spacer and adjacent to said source/drain region.

14. (original) The device of claim 9, wherein a width of said oxide spacer is not larger than a width of said spacer.